OpenMP* SIMD Programming

Dr.-Ing. Michael Klemm
Senior Application Engineer
Software and Services Group
(michael.klemm@intel.com)

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Levels of Parallelism

<table>
<thead>
<tr>
<th>Level</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cluster</td>
<td>Group of computers communicating through fast interconnect</td>
</tr>
<tr>
<td>Coprocessors/Accelerators</td>
<td>Special compute devices attached to the local node through special interconnect</td>
</tr>
<tr>
<td>Node</td>
<td>Group of processors communicating through shared memory</td>
</tr>
<tr>
<td>Socket</td>
<td>Group of cores communicating through shared cache</td>
</tr>
<tr>
<td>Core</td>
<td>Group of functional units communicating through registers</td>
</tr>
<tr>
<td>Hyper-Threads</td>
<td>Group of thread contexts sharing functional units</td>
</tr>
<tr>
<td>Superscalar</td>
<td>Group of instructions sharing functional units</td>
</tr>
<tr>
<td>Pipeline</td>
<td>Sequence of instructions sharing functional units</td>
</tr>
<tr>
<td>Vector</td>
<td>Single instruction using multiple functional units</td>
</tr>
</tbody>
</table>
SIMD on Intel® Architecture

- **SSE**
  - 128 bit
  - 2 x DP
  - 4 x SP

- **AVX**
  - 256 bit
  - 4 x DP
  - 8 x SP

- **MIC AVX-512**
  - 512 bit
  - 8 x DP
  - 16 x SP
More Powerful SIMD Units

• SIMD instructions become more powerful on the Intel® Xeon Phi™ Processor

\[ \text{vaddpd dest, source1, source2} \]

\[
\begin{array}{cccccccc}
  a7 & a6 & a5 & a4 & a3 & a2 & a1 & a0 \\
\end{array}
\]

\[
\begin{array}{cccccccc}
  b7 & b6 & b5 & b4 & b3 & b2 & b1 & b0 \\
\end{array}
\]

\[ + \]

\[
\begin{array}{cccccccc}
  a7+b7 & a6+b6 & a5+b5 & a4+b4 & a3+b3 & a2+b2 & a1+b1 & a0+b0 \\
\end{array}
\]

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More Powerful SIMD Units

- SIMD instructions become more powerful on the Intel® Xeon Phi™ Processor

```
vfmadd213pd source1, source2, source3
```

<table>
<thead>
<tr>
<th>a7</th>
<th>a6</th>
<th>a5</th>
<th>a4</th>
<th>a3</th>
<th>a2</th>
<th>a1</th>
<th>a0</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>b6</td>
<td>b5</td>
<td>b4</td>
<td>b3</td>
<td>b2</td>
<td>b1</td>
<td>b0</td>
</tr>
<tr>
<td>c7</td>
<td>c6</td>
<td>c5</td>
<td>c4</td>
<td>c3</td>
<td>c2</td>
<td>c1</td>
<td>c0</td>
</tr>
</tbody>
</table>

```
dest = a7*b7 +c7 + a6*b6 +c6 + a5*b5 +c5 + a4*b4 +c4 + a3*b3 +c3 + a2*b2 +c2 + a1*b1 +c1 + a0*b0 +c0
```
More Powerful SIMD Units

- SIMD instructions become more powerful on the Intel® Xeon Phi™ Processor

```
vaddpd dest{k1}, source2, source3
```

```
+  

=  
```

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More Powerful SIMD Units

- SIMD instructions become more powerful on the Intel® Xeon Phi™ Processor

```
vmovapd dest, source{daci}
```

```
512 bit
```

```
av 7 a6 a5 a4 a3 a2 a1 a0
```

**source**

```
swizzle
```

```
av 7 a4 a6 a5 a3 a0 a2 a1
```

**“tmp”**

```
move
```

```
av 7 a4 a6 a5 a3 a0 a2 a1
```

**dest**

SOFTWARE AND SERVICES
• Auto vectorization only helps in some cases
  • Increased complexity of instructions makes it hard for the compiler to select proper instructions
  • Code pattern needs to be recognized by the compiler
  • Precision requirements often inhibit SIMD code gen
• Example: Intel® Composer XE
  • -vec (automatically enabled with –O2)
  • -qopt-report
Why Auto-vectorizers Fail

- Data dependencies
- Other potential reasons
  - Alignment
  - Function calls in loop block
  - Complex control flow / conditional branches
  - Loop not “countable”
    - E.g. upper bound not a runtime constant
  - Mixed data types
  - Non-unit stride between elements
  - Loop body too complex (register pressure)
  - Vectorization seems inefficient
- Many more ... but less likely to occur
Example: Loop not Countable

- “Loop not Countable” plus “Assumed Dependencies”

```c
typedef struct {
    float* data;
    size_t size;
} vec_t;

void vec_eltwise_product(vec_t* a, vec_t* b, vec_t* c) {
    size_t i;
    for (i = 0; i < a->size; i++) {
        c->data[i] = a->data[i] * b->data[i];
    }
}
```
In a Time before OpenMP 4.0

• Programmers had to rely on auto-vectorization...
• ... or to use vendor-specific extensions
  • Programming models (e.g., Intel® Cilk™ Plus)
  • Compiler pragmas (e.g., #pragma vector)
  • Low-level constructs (e.g., _mm_add_pd())

```c
#pragma omp parallel for
#pragma vector always
#pragma ivdep
for (int i = 0; i < N; i++) {
    a[i] = b[i] + ...;
}
```

You need to trust the compiler to do the “right” thing.
OpenMP SIMD Loop Construct

- Vectorize a loop nest
  - Cut loop into chunks that fit a SIMD vector register
  - No parallelization of the loop body

- Syntax (C/C++)
  #pragma omp simd [clause[[], clause],...]
  for-loops

- Syntax (Fortran)
  !$omp simd [clause[[], clause],...]
  do-loops
Example

```c
void sprod(float *a, float *b, int n) {
    float sum = 0.0f;
    #pragma omp simd reduction(+:sum)
    for (int k=0; k<n; k++)
        sum += a[k] * b[k];
    return sum;
}
```

**vectorize**

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Data Sharing Clauses

- **private** (*var-list)*:
  Uninitialized vectors for variables in *var-list*

  ![Example](x: 42 \rightarrow ? ? ? ?)

- **firstprivate** (*var-list)*:
  Initialized vectors for variables in *var-list*

  ![Example](x: 42 \rightarrow 42 \ 42 \ 42 \ 42)

- **reduction** (*op:var-list)*:
  Create private variables for *var-list* and apply reduction operator *op* at the end of the construct

  ![Example](12 \ 5 \ 8 \ 17 \rightarrow x: 42)
SIMD Loop Clauses

- **safelen (length)**
  - Maximum number of iterations that can run concurrently without breaking a dependence
  - In practice, maximum vector length

- **linear (list[:linear-step])**
  - The variable’s value is in relationship with the iteration number
    \[ x_i = x_{orig} + i \times \text{linear-step} \]

- **aligned (list[:alignment])**
  - Specifies that the list items have a given alignment
  - Default is alignment for the architecture

- **collapse (n)**
Loop-Carried Dependencies

• Dependencies may occur across loop iterations
  • Loop-carried dependency

• The following code contains such a dependency:

```c
void lcd_ex(float* a, float* b, size_t n, float c1, float c2) {
    size_t i;
    for (i = 0; i < n; i++) {
        a[i] = c1 * a[i + 17] + c2 * b[i];
    }
}
```

• Some iterations of the loop have to complete before the next iteration can run
  • Simple trick: can you reverse the loop w/o getting wrong results?
Loop-Carried Dependencies

• Can we parallelize or vectorize the loop?
  • Parallelization: no (except for very specific loop schedules)
  • Vectorization: yes (if vector length is shorter than any distance of any dependency)
SIMD Worksharing Construct

- Parallelize and vectorize a loop nest
  - Distribute a loop’s iteration space across a thread team
  - Subdivide loop chunks to fit a SIMD vector register

- Syntax (C/C++)
  ```
  #pragma omp for simd [clause[, clause],...]
  for-loops
  ```

- Syntax (Fortran)
  ```
  !$omp do simd [clause[, clause],...]
  do-loops
  ```
```c
void sprod(float *a, float *b, int n) {
    float sum = 0.0f;
    #pragma omp for simd reduction(+:sum)
    for (int k=0; k<n; k++)
        sum += a[k] * b[k];
    return sum;
}
```
void sprod(float *a, float *b, int n) {
    float sum = 0.0f;
    #pragma omp for simd reduction(+:sum) \
        schedule(static, 5)
    for (int k=0; k<n; k++)
        sum += a[k] * b[k];
    return sum;
}

• You should choose chunk sizes that are multiples of the SIMD length
  • Remainder loops are not triggered
  • Likely better performance
• In the above example ...
  • and AVX2, the code will only execute the remainder loop!
  • and SSE, the code will have one iteration in the SIMD loop plus one in the remainder loop!
### Schedule Modifiers

```c
void sprod(float *a, float *b, int n) {
    float sum = 0.0f;
    #pragma omp for simd reduction(+:sum) \ 
        schedule(simd:static, 5)
    for (int k=0; k<n; k++)
        sum += a[k] * b[k];
    return sum;
}
```

- The new simd modifier automatically adjusts the chunk size to match it with the length of the SIMD register.
  - New chunk size becomes \( \frac{\text{chunksz}}{\text{simdlen}} \times \text{simdlen} \)
  - AVX2: new chunk size will be 8
  - SSE: new chunk size will be 8
SIMD Function Vectorization

float min(float a, float b) {
    return a < b ? a : b;
}

float distsq(float x, float y) {
    return (x - y) * (x - y);
}

void example() {
    #pragma omp parallel for simd
    for (i=0; i<N; i++) {
        d[i] = min(distsq(a[i], b[i]), c[i]);
    }
}
SIMD Function Vectorization

• Declare one or more functions to be compiled for calls from a SIMD-parallel loop

• Syntax (C/C++):
  
  ```
  #pragma omp declare simd [clause[, clause],...]
  [pragma omp declare simd [clause[, clause],...]]
  [.....]
  function-definition-or-declaration
  ```

• Syntax (Fortran):
  
  ```
  !$omp declare simd (proc-name-list)
  ```
#pragma omp declare simd
float min(float a, float b) {
    return a < b ? a : b;
}

#pragma omp declare simd
float distsq(float x, float y) {
    return (x - y) * (x - y);
}

void example() {
    #pragma omp parallel for simd
    for (i=0; i<N; i++) {
        d[i] = min(distsq(a[i], b[i]), c[i]);
    }
}

vec8 min_v(vec8 a, vec8 b) {
    return a < b ? a : b;
}

vec8 distsq_v(vec8 x, vec8 y) {
    return (x - y) * (x - y);
}

vd = min_v(distsq_v(va, vb, vc))
SIMD Function Vectorization

• **simdlen** (*length*)
  • generate function to support a given vector length
• **uniform** (*argument-list*)
  • argument has a constant value between the iterations of a given loop
• **inbranch**
  • function always called from inside an if statement
• **notinbranch**
  • function never called from inside an if statement
• **linear** (*argument-list[:linear-step]*)
• **aligned** (*argument-list[:alignment]*)
• **reduction** (*operator:list*)

SOFTWARE AND SERVICES
#pragma omp declare simd inbranch

```c
float do_stuff(float x) {
    /* do something */
    return x * 2.0;
}
```

```c
void example() {
    #pragma omp simd
    for (int i = 0; i < N; i++)
        if (a[i] < 0.0)
            b[i] = do_stuff(a[i]);
}
```

```c
vec8 do_stuff_v(vec8 x, mask m) {
    /* do something */
    vmulpd x{m}, 2.0, tmp
    return tmp;
}
```

```c
for (int i = 0; i < N; i+=8) {
    vcmp_lt &a[i], 0.0, mask
    b[i] = do_stuff_v(&a[i], mask);
}
```